REMARKS

Claim Objections

Claim 1 has been amended to address the objections raised in the Office Action.

Rejection of Claims 1-9 and 11 Under 35 U.S.C. §102(e) based on *Ishitsuka et al.* (U.S. Patent No. 6,242,323)

The rejection of claims 1-6 will first be addressed.

The invention of amended claim 1 includes a semiconductor device having a trench element separation region that includes a trench formed in a surface of a semiconductor substrate, and that isolates separate semiconductor elements. The trench element separation region also includes an oxide film formed on inner walls of the trench and a trench filling insulating material filling the trench and having edges above the inner walls of the trench. The edges of the trench filling insulating material are defined by side edges of a sacrificial layer formed by an etching process including a neutral radical. Inner wall edges in a top section of the trench and the edges of the trench filling insulating material are formed so as to be essentially located on the same plane.

As is well established, anticipation requires the presence of a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.[1]

The cited reference does not show a trench filling insulating material defined by side edges of a sacrificial layer formed by an etching process including a neutral radical. Accordingly, all limitations are not shown and this ground of rejection is traversed.

The invention of amended claim 1 is substantially different than the structure of the cited reference, which appears no different than Applicant's admitted prior art. The semiconductor device of claim 1 has a trench filling insulating material with an edge that is clearly different than, and unobvious over, the cited reference *Ishitsuka et al.*

As recited in claim 1, a trench filling insulating material edge is defined by side edges of a sacrificial layer formed by an etching process including a neutral radical. Particular examples

[1] See Lindemann Maschinenefabrick GmbH v. American Hoist & Derrick Col., 221 USPQ 481, 485 (Fed. Cir. 1984).

of such a structure, and resulting possible advantages, were clearly recited in the Specification.[2] Applicant's invention is thus in sharp contrast to *Ishitsuka et al.* edge, formed by a step that in no way shows or suggests Applicant's clearly defined neutral radical etching process.[3] In fact, *Ishitsuka et al.* appears no different than Applicant's conventional approach described in the background art.[4]

In summary, Applicant's have demonstrated clear differences between a trench filling insulating material edge according to claim 1, and an edge of a deposited silicon oxide film in the cited reference. When such differences are taken into account, the cited reference does not show "edges of the trench filling insulating material are defined by side edges of a sacrificial layer formed by an etching process including a neutral radical." Accordingly, the reference cannot anticipate the claim.

For these reasons this ground for rejection is traversed.

The rejection of claims 7-9 and 11 will now be addressed.

Amended claim 7 is directed to a semiconductor device with a trench element separation region. The including a trench formed in a surface of a semiconductor substrate, the trench element separation region isolating a first doped channel layer of a first insulated gate field effect transistor (IGFET) from a second doped channel layer of a second IGFET. An oxide film formed on inner walls of the trench. In addition, a trench filling insulating material fills the trench and has edges above the inner walls of the trench defined by side edges of a sacrificial layer formed by an etching process including a neutral radical. Inner wall edges in a top section of the trench and the edges of the trench filling insulating material are formed so as to be essentially located on the same plane.

To the extent that this ground for rejection relies on the reference *Ishitsuka et al.*, the comments set forth above for claim 1 are incorporated by reference herein. Namely, that the

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[2] See the Specification, FIG. 3 and Page 16, Lines 9-17, which indicate that a silicon nitride film 3a results by a "pullback" process that can pull back an edge. Thus, a sacrificial layer edge according to Applicant's claim 1 can be further back and more precise than conventional approaches.

[3] See, for example, *Ishitsuka et al.*, FIG. 13 and description at Col. 23, Lines 23-44, which describes etching a silicon nitride film without any details whatsoever.

[4] See the Specification, FIGS. 10(a) to 10(d), which simply patterns a silicon nitride film 103, without a neutral radical etch.

reference does not show a trench filling insulating material edge defined by side edges of a sacrificial layer formed by an etching process that includes a neutral radical.

Rejection of Claims 7 and 10 Under 35 U.S.C. §102(e) based on *Bhakta et al.* (U.S. Patent No. 6,258,697)

The cited reference *Bhakta et al.* does not show all the limitations of claim 7. The reference *Bhakta et al.* fails to show a trench filling insulating material edge defined by side edges of a sacrificial layer, as recited in claim 7.

Bhakta et al. discloses a semiconductor device having a trench that is filled with a filling material. However, edges of a filling material are not defined by side edges of a sacrificial layer, but rather an oxide liner layer.[5]

For this reason, this ground of rejection is traversed.

Claims 1, 3, 7 and 9 have been amended. Claims 2, 4 and 8 have been cancelled. The present claims 1, 3, 5-7, and 9-11 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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[5] See *Bhakta et al.*, FIG. 3D, which shows that edges of trench filling material 46 are defined by oxide line 42, and not a polish stop layer 34 (argued to correspond to Applicant's sacrificial layer).

Version With Markings to Show Changes Made

In the Claims.

1. (Amended) A semiconductor device, comprising:

a trench element separation region including a trench formed in a surface of a semiconductor substrate, the trench element separation region isolating separate semiconductor elements;

an oxide film formed on inner walls of the trench;

a trench filling insulating material filling the trench and having edges above the inner walls of the trench **that are defined by side edges of a sacrificial layer formed by an etching process including a neutral radical**; and

wherein **inner wall edges in** a top section of the trench and the edges of the trench filling insulating material are formed so as to be essentially located on the same plane.

Please cancel claim 2.

3. (Amended) The semiconductor device of claim **1** **[2]**, wherein the sacrificial layer is a silicon nitride film.

Please cancel claim 4.

7. (Amended) A semiconductor device, comprising:

a trench element separation region including a trench formed in a surface of a semiconductor substrate, the trench element separation region isolating a first doped channel layer of a first insulated gate field effect transistor (IGFET) from a second doped channel layer of a second IGFET;

an oxide film formed on inner walls of the trench;

a trench filling insulating material filling the trench and having edges above the inner walls of the trench **defined by side edges of a sacrificial layer formed by an etching process including a neutral radical**; and

wherein inner wall edges in a top section of the trench and the edges of the trench filling insulating material are formed so as to be essentially located on the same plane.

Please cancel claim 8.

9. (Amended) The semiconductor device of claim 7 **[8]**, wherein:

the **[side edges of the sacrificial layer are formed by an]** etching process **includes [including]** a fluorine radical.